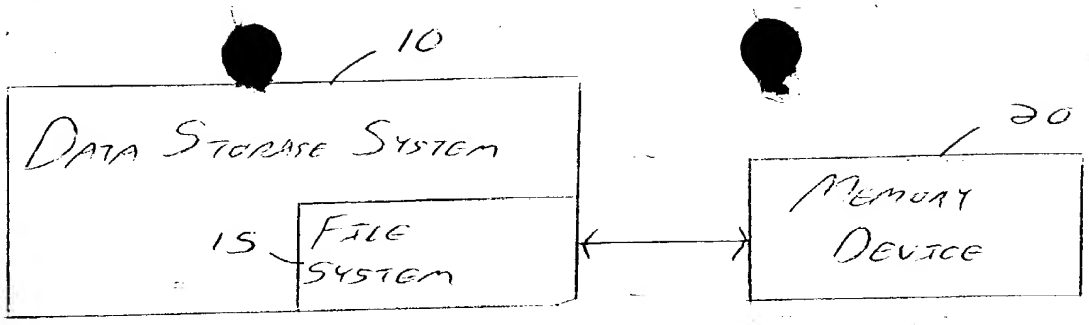

FIGURE 1

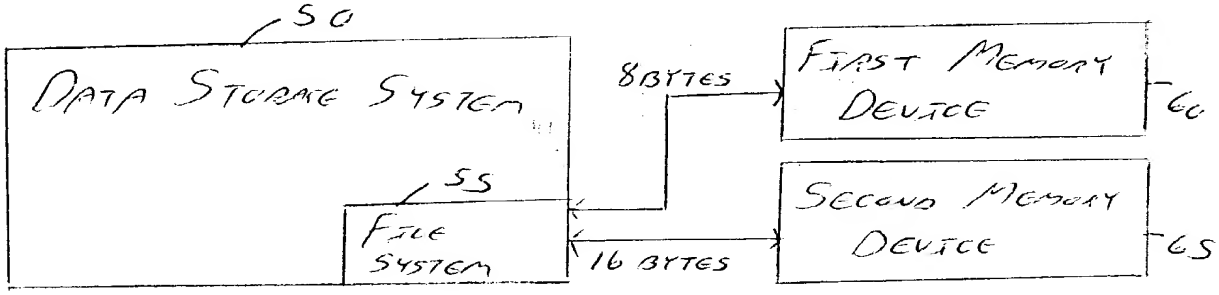

FIGURE 3

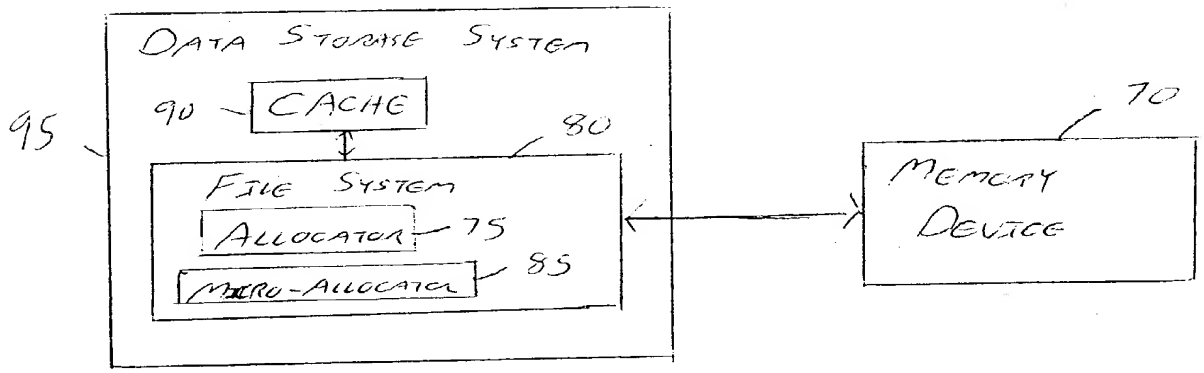

FIGURE 5

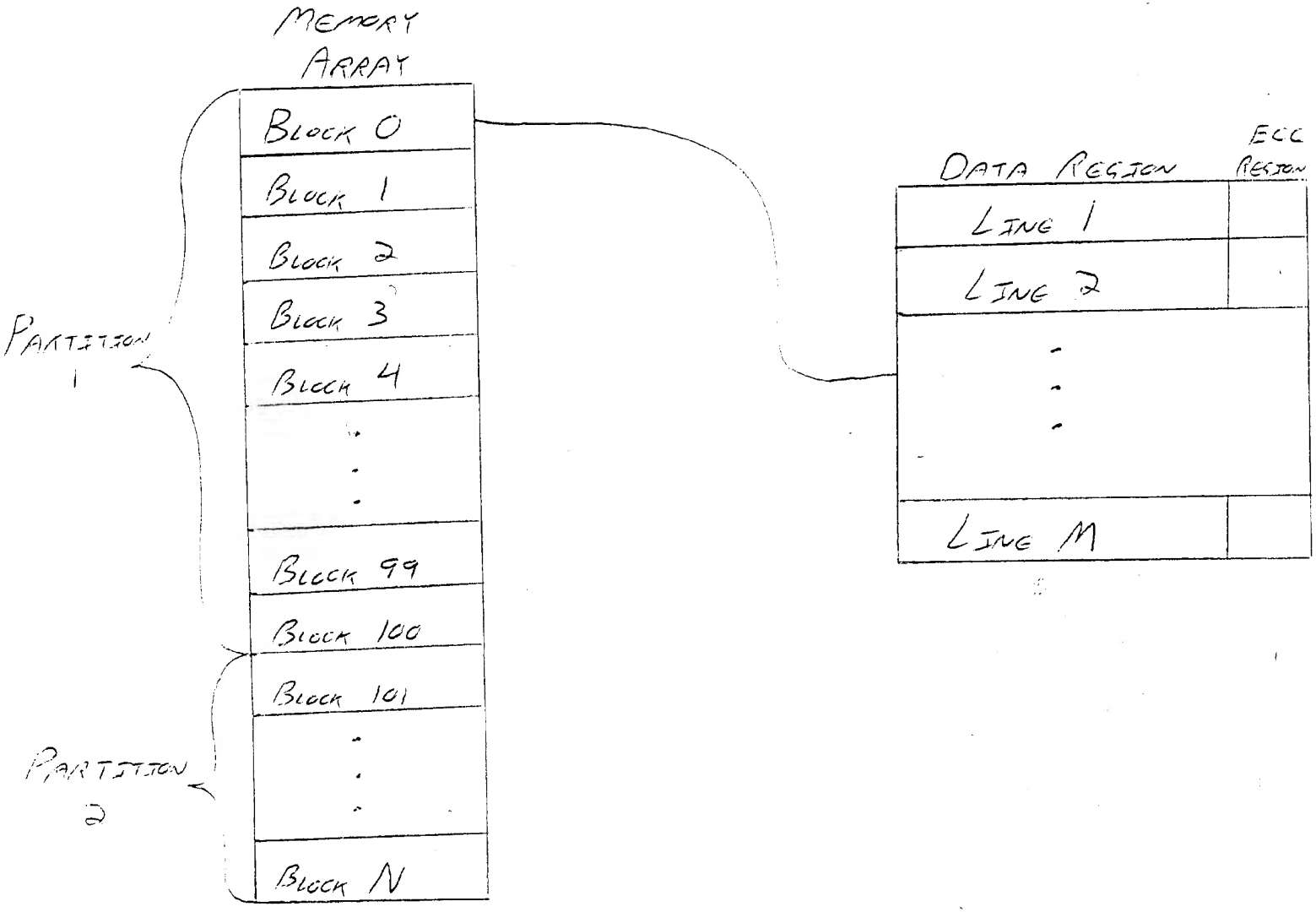
MEMORY ARRAY
BLOCK 0
BLOCK 1
BLOCK 2
BLOCK 3
BLOCK 4
BLOCK 99
BLOCK 100
BLOCK 101
BLOCK N
PARTITION 1
PARTITION 2
DATA REGION
ECC REGION
LINE 1
LINE 2
LINE M

FIGURE 2

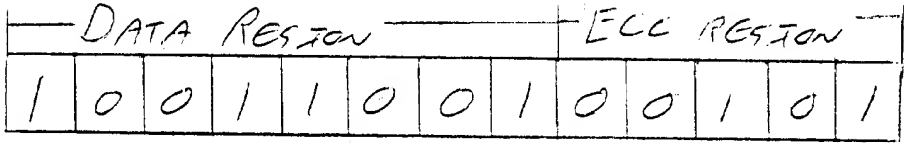

FIGURE 4A

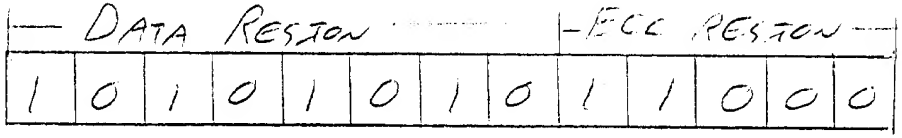

FIGURE 4B

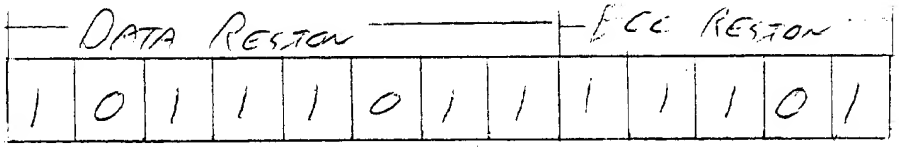

FIGURE 4C

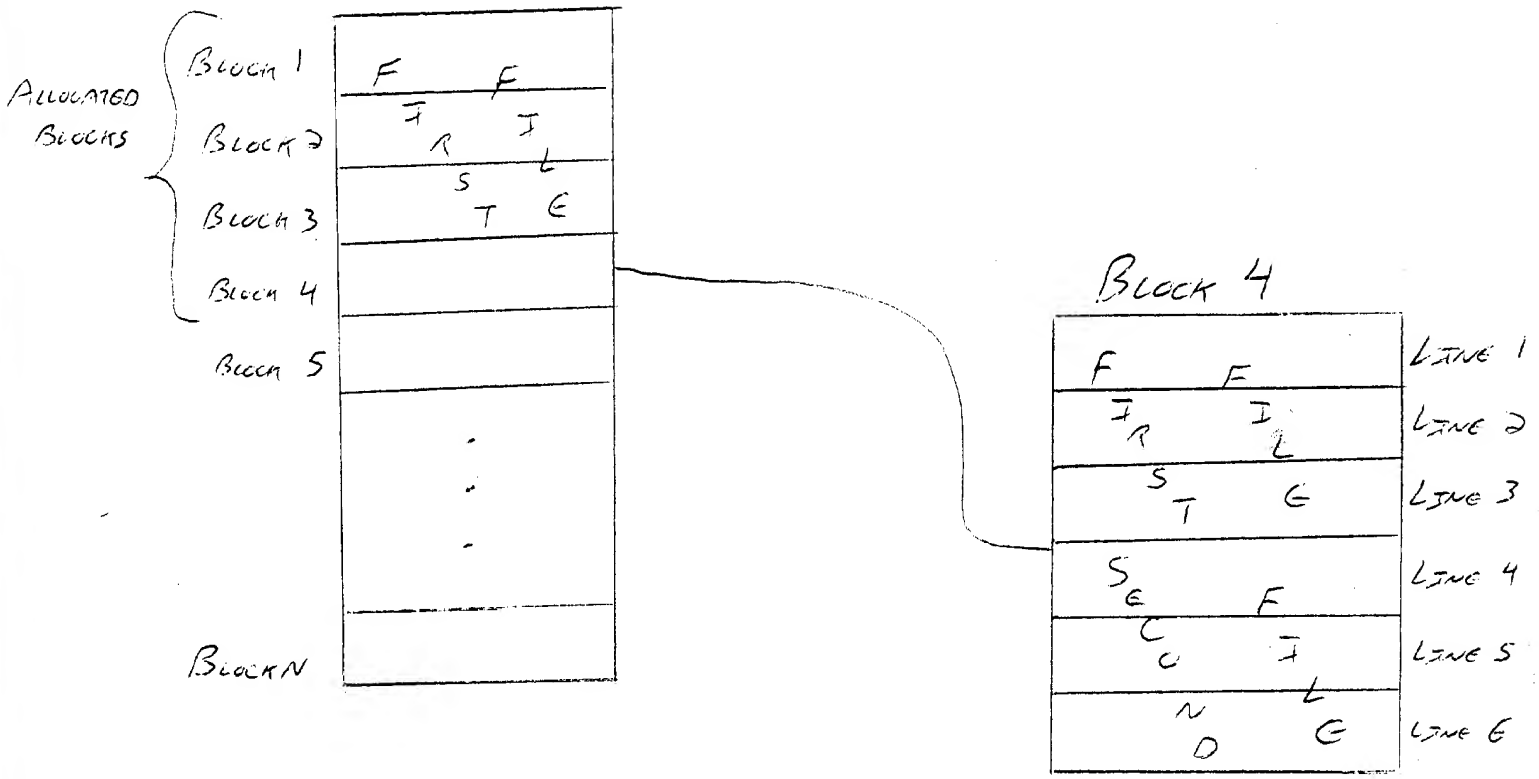
ALLOCATED BLOCKS
BLOCK 1
BLOCK 2
BLOCK 3
BLOCK 4
BLOCK 5
BLOCK N
BLOCK 4
LINE 1
LINE 2
LINE 3
LINE 4
LINE 5
LINE 6

FIGURE 6

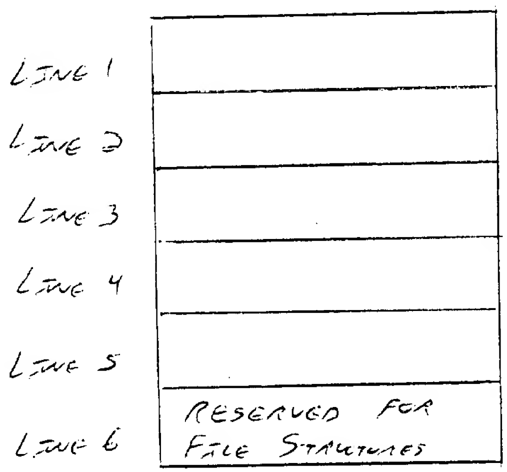

FIGURE 7A

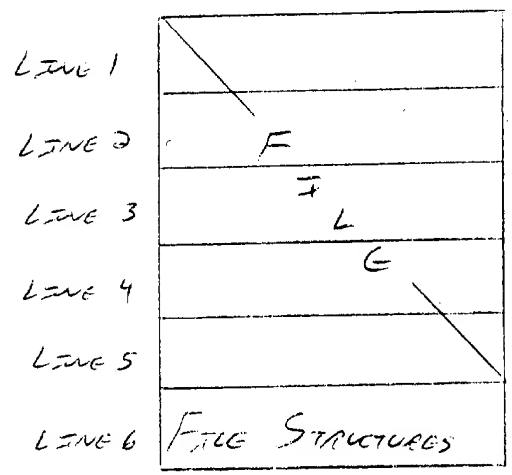

FIGURE 7B

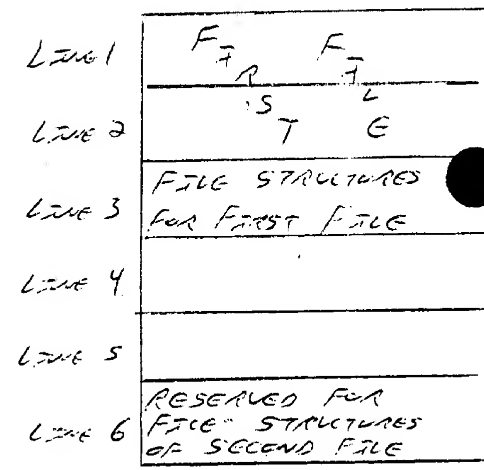

FIGURE 7C

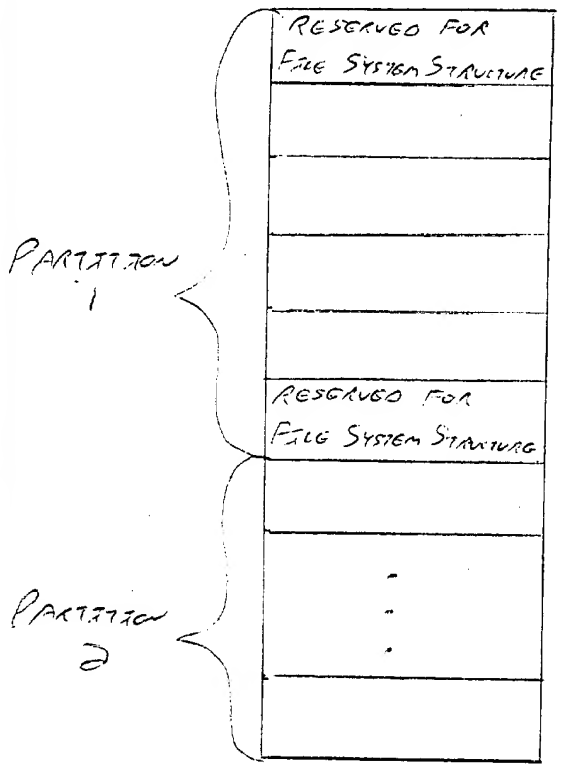

FIGURE 8A

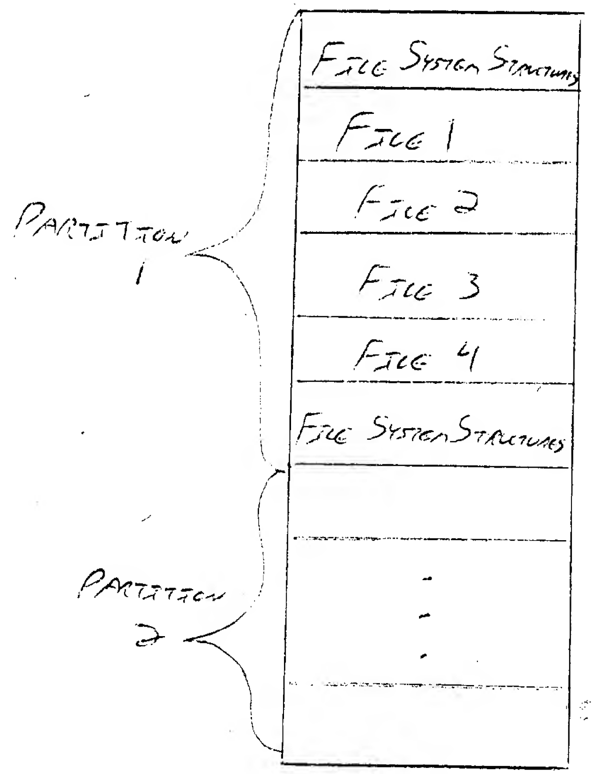

FIGURE 8B

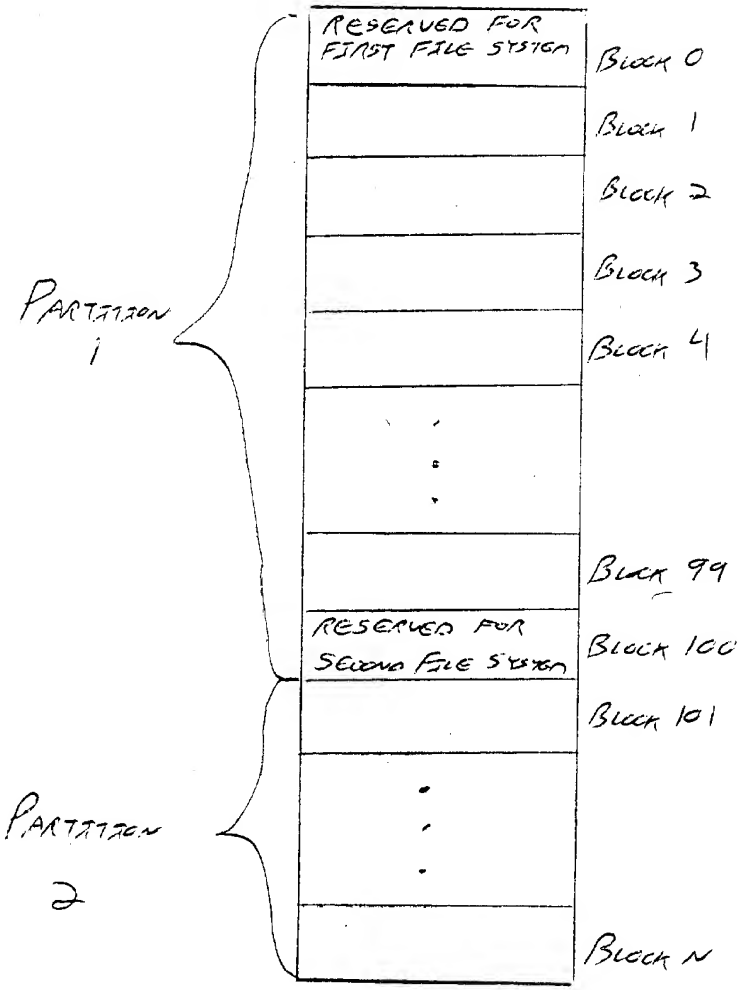

FIGURE 9A

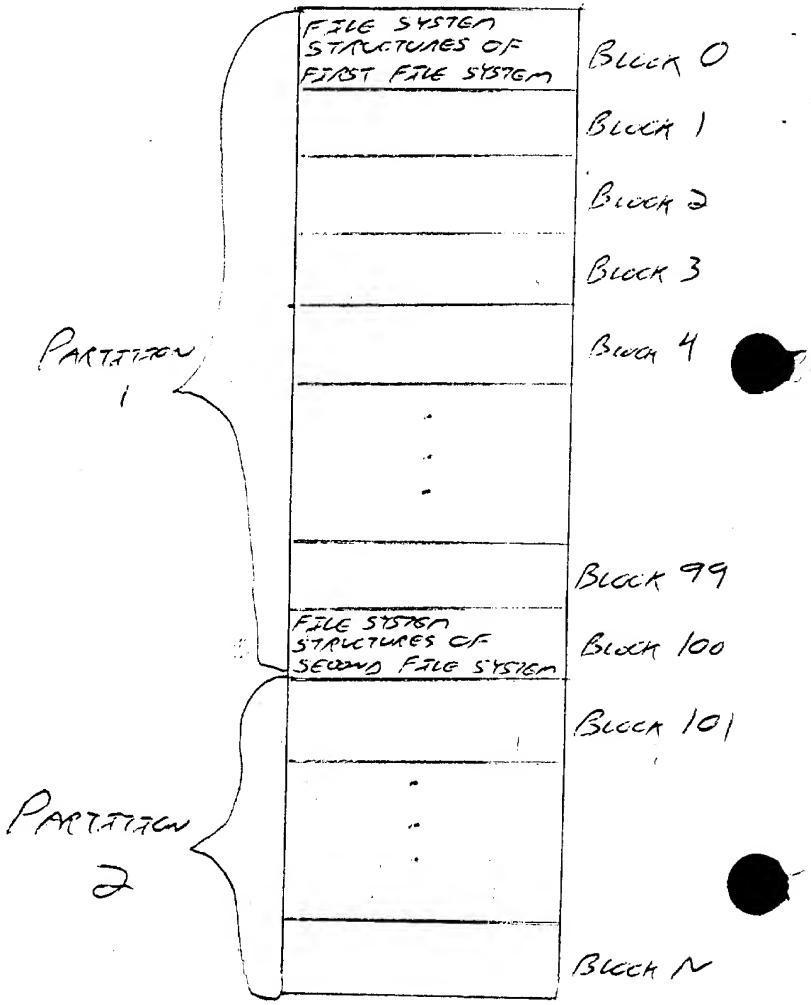

FIGURE 9B

1	1	0	1
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0

FIGURE 10A

1	1	0	1
1	1	1	0
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0

FIGURE 10B

1	1	0	1
1	1	1	0
0	0	0	0
0	1	1	0
1	0	0	1
0	0	0	0

FIGURE 10C

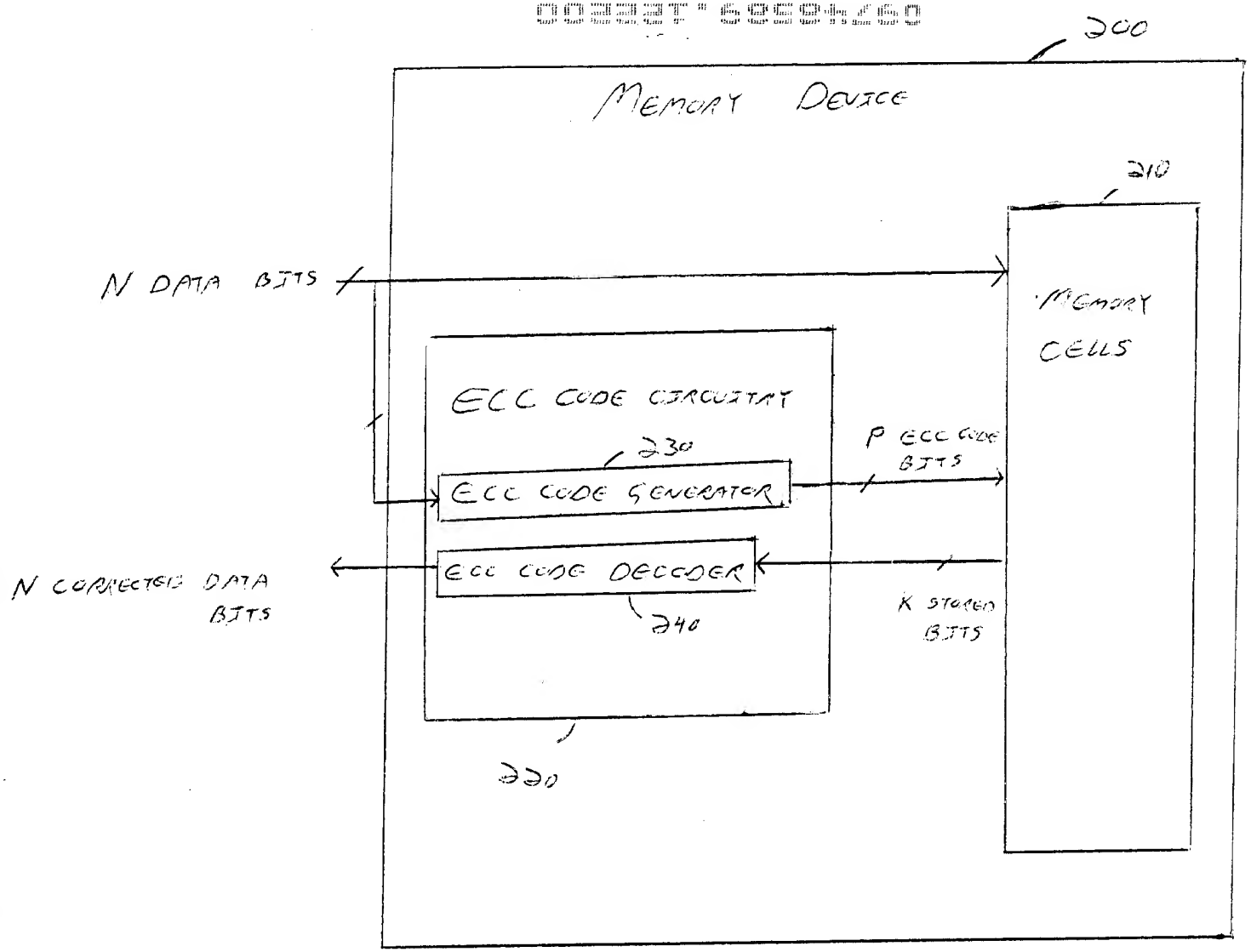
200
MEMORY DEVICE
210
N DATA BITS
MEMORY CELLS
ECC CODE CIRCUITAT
230
ECC CODE GENERATOR
P ECC CODE BITS
N CORRECTED DATA BITS
ECC CODE DECODER
K STORED BITS
240
220

FIGURE 11